CLAIMS

What is claimed is:

1. A method for correcting antenna violations in high-density integrated circuits, the method comprises:

determining location of an antenna violation within a layout of a high-density integrated circuit;

determining an affected input of a cell of the high-density integrated circuit based on the location of the antenna error;

identifying an available charge protection element; and

logically coupling the available charge protection element to the affected input of the cell.

2. The method of claim 1 further comprises performing a rerouting algorithm to physically connect the available charge protection element to the affected input of the cell.

3. The method of claim 1, wherein the determining the affected input further comprises:

identifying the cell based on the location of the antenna violation;

identifying circuitry within the cell corresponding to the location of the antenna violation;

determining whether the circuitry includes an element with an input; and

when the circuitry includes the element with the input, identifying the affected input as the input of the element within the circuitry.

4. The method of claim 1, wherein the identifying the available charge element further comprises at least one of:

determining a closest charge protection element to the affected input; and

determining a charge protection element along a wire coupled to the affected input.

5. The method of claim 1 further comprises, prior to determining location of antenna violation:

performing a place and route algorithm to position cells to form an initial layout of the high-density integrated circuit;

determining available space within the initial layout; placing at least one charge protection element within the available space; and

re-performing the place and route algorithm to produce the layout to include the coupling of the available charge protection element to the affected input of the cell.

6. The method of claim 1, wherein the charge protection element comprises at least one of: a diode, a transistor, and a surge protector.

7. A method for correcting antenna violations in high-density integrated circuits, the method comprises:

interpreting an integrated circuit error report to obtain error coordinates;

determining a cell of the integrated circuit based on the error coordinates and a design exchange format file;

determining error position within the cell based on the error coordinates;

determining an affected input of the cell based on the error position and a library exchange file; and

identifying an available charge protection element; and logically coupling the available charge protection element to the affected input of the cell.

8. The method of claim 7 further comprises:

executing a design rule checking algorithm to obtain the integrated circuit error report.

9. The method of claim 7 further comprises:

generating an updated design exchange format file; and

executing a routing algorithm to physically connect the available charge protection element to the affected input of the cell.

10. The method of claim 7, wherein the identifying the available charge element further comprises at least one of:

determining closest element to the affected input; and

determining element along a wire coupled to the affected input.

11. The method of claim 7, wherein the determining the affected input of the cell based on the error position and the library exchange file further comprises:

interpreting the library exchange file to determine inputs and outputs of the cell;

determining location of the inputs within the cell; and

identifying one of the inputs as the affected input based on the location of the one of the inputs being proximal to the error position.

12. The method of claim 7 further comprises, prior to interpreting an integrated circuit error report:

performing a place and route algorithm to position cells to form an initial layout of the integrated circuit;

determining available space within the initial layout;

placing at least one charge protection element within the available space; and

re-performing the place and route algorithm to produce a layout of the integrated circuit to include the coupling of the available charge protection element to the affected input of the cell.

13. The method of claim 7, wherein the charge protection element comprises at least one of: a diode, a transistor, and

a surge protector.

14. An integrated circuit comprises:
a plurality of cells arranged to form an integrated circuit layout; and

a plurality of charge protection elements placed within available space of the integrated circuit layout, wherein at least one of the plurality of charge protection elements is coupled to at least one of the plurality of cells by:

determining location of an antenna violation within the integrated circuit layout;

determining an affected input of the at least one of the plurality of cells based on the location of the antenna error;

identifying the at least one of the charge protection elements; and

coupling the at least one of the plurality of charge protection elements to the affected input of the at least one of the plurality of cells.

15. The integrated circuit of claim 14, wherein the coupling the at least one of the plurality of charge protection elements to the affected input of the at least one of the plurality of cells further comprises performing a rerouting algorithm to physically connect the at least one of the plurality of charge protection elements to the affected input of the at least one of the plurality of cells.

16. The integrated circuit of claim 14, wherein the determining the affected input further comprises:

identifying the at least one of the plurality of cells based on the location of the antenna violation;

identifying circuitry within the at least one of the plurality of cells corresponding to the location of the antenna violation;

determining whether the circuitry includes an element

with an input; and

when the circuitry includes the element with the input, identifying the affected input as the input of the element within the circuitry.

17. The integrated circuit of claim 14, wherein the identifying the at least one of the plurality of charge protection elements further comprises at least one of:

determining a closest one of the plurality of charge protection elements to the affected input; and

determining a charge protection element of the plurality of charge protection elements that is along a wire coupled to the affected input.

18. The integrated circuit of claim 14 further comprises, prior to determining location of antenna violation:

performing a place and route algorithm to position the plurality of cells to form an initial layout of the integrated circuit;

determining the available space within the initial layout;

placing the plurality of charge protection elements within the available space; and

re-performing the place and route algorithm to produce the integrated circuit layout to include the coupling of the at least one of the plurality of charge protection elements to the affected input of the at least one of the plurality of cells.

19. The integrated circuit of claim 14, wherein each of the plurality of charge protection elements comprises at least one of: a diode, a transistor, and a surge protector.

20. An integrated circuit comprises:

a plurality of cells arranged to form an integrated circuit layout; and

a plurality of charge protection elements placed within available space of the integrated circuit layout, wherein at least one of the plurality of charge protection elements is coupled to at least one of the plurality of cells by:

interpreting an integrated circuit error report to obtain error coordinates;

determining a cell of the plurality of cells based on the error coordinates and a design exchange format file;

determining error position within the cell based on the error coordinates;

determining an affected input of the cell based on the error position and a library exchange file;

identifying an available charge protection element of the plurality of charge protection elements; and

coupling the available charge protection element to the affected input of the cell.

21. The integrated circuit of claim 20, wherein the coupling the available charge protection element to the affected input of the cell further comprises:

executing a design rule checking algorithm to obtain the integrated circuit error report.

22. The integrated circuit of claim 20, wherein the coupling the available charge protection element to the affected input of the cell further comprises:

generating an updated design exchange format file; and

executing a routing algorithm to physically connect the available charge protection element to the affected input of the cell.

23. The integrated circuit of claim 20, wherein the identifying the available charge element further comprises at least one of:

determining a closest one of the plurality of charge

protection elements to the affected input; and

determining a charge protection element of the plurality of charge protection elements along a wire coupled to the affected input.

24. The integrated circuit of claim 20, wherein the determining the affected input of the cell based on the error position and the library exchange file further comprises:

interpreting the library exchange file to determine inputs and outputs of the cell;

determining location of the inputs within the cell; and

identifying one of the inputs as the affected input based on the location of the one of the inputs being proximal to the error position.

25. The integrated circuit of claim 20, wherein the coupling the available charge protection element to the affected input of the cell further comprises, prior to interpreting an integrated circuit error report:

performing a place and route algorithm to position the plurality of cells to form an initial layout of the integrated circuit;

determining the available space within the initial layout;

placing the plurality of charge protection elements within the available space; and

re-performing the place and route algorithm to produce the integrated circuit layout to include the coupling of the available charge protection element to the affected input of the cell.

26. The integrated circuit of claim 20, wherein each of the plurality of charge protection elements comprises at least one of: a diode, a transistor, and a surge protector.

27. A method for designing a high-density integrated circuits, the method comprises:

performing a place and route algorithm to position cells to form an initial layout of the high-density integrated circuit;

determining available space within the initial layout; placing at least one charge protection element within the available space;

determining location of an antenna violation within the initial layout;

determining an affected input of one of the cells of the high-density integrated circuit based on the location of the antenna error;

identifying an available charge protection element of the at least one charge protection element; and

re-performing the place and route algorithm to produce a layout to include the coupling of the available charge protection element to the affected input of the one of the cells.

28. The method of claim 27, wherein the determining the affected input further comprises:

identifying the one of the cells based on the location of the antenna violation;

identifying circuitry within the one of the cells corresponding to the location of the antenna violation;

determining whether the circuitry includes an element with an input; and

when the circuitry includes the element with the input, identifying the affected input as the input of the element within the circuitry.

29. The method of claim 27, wherein the identifying the available charge element further comprises at least one of:

determining a closest charge protection element to the affected input; and

determining a charge protection element along a wire coupled to the affected input.

30. The method of claim 27, wherein the charge protection element comprises at least one of: a diode, a transistor, and a surge protector.

31. An integrated circuit comprises:

a plurality of cells arranged to form an integrated circuit layout; and

a plurality of charge protection elements placed within available space of the integrated circuit layout, wherein at least one of the plurality of charge protection elements is coupled to at least one of the plurality of cells by:

performing a place and route algorithm to position the plurality of cells to form an initial layout of the integrated circuit;

determining available space within the initial layout;

placing at least one charge protection element of the plurality of charge protection elements within the available space;

determining location of an antenna violation within the initial layout;

determining an affected input of a cell of the plurality of cells based on the location of the antenna error;

identifying an available charge protection element of the at least one charge protection element; and

re-performing the place and route algorithm to produce the integrated circuit layout to include the coupling of the available charge protection element to the affected input of the cell.

32. The integrated circuit of claim 31, wherein the determining the affected input further comprises:

identifying the cell based on the location of the antenna violation;

identifying circuitry within the cell corresponding to the location of the antenna violation;

determining whether the circuitry includes an element with an input; and

when the circuitry includes the element with the input, identifying the affected input as the input of the element within the circuitry.

33. The integrated circuit of claim 31, wherein the identifying the available charge element further comprises at least one of:

determining a closest charge protection element to the affected input; and

determining a charge protection element along a wire coupled to the affected input.

34. The integrated circuit of claim 31, wherein each of the plurality of charge protection elements comprises at least one of: a diode, a transistor, and a surge protector.